*Cl* **45** *SC* **45.2.3.87c.3** *P* **36** *L* **20** # 242

Slavick, Jeff — Broadcom

*Comment Type* **TR** *Comment Status* **R** *Registers effect*

There is no reflection of what the current operating mode of OAM. 3.2348.1 only takes affect after a pmd_reset, so how do you tell if the current state of the enable bit represents the opereation state?

*SuggestedRemedy*

Add a new BASE-U OAM status field that reflects the current operating state of OAM mode.

*Response* *Response Status* **U**

REJECT.
According to 166.11 (with references to 115.9), BASE-U OAM channel is established when both link partners transmits PHD.CAP.OAM = 1, which indicates both partners have the optional ability of OAM channel and it is enabled. The status of the PHD operation is reported to any attached STA by the PHD lock status bit (3.2349.10) and the local and remote PHD reception status bits (3.2349.11 and 3.2349.12). Once the PHD bidirectional communication is indicated reliable, register BASE-U OAM enable (3.2348.1) and Remote BASE-U OAM ability (3.2349.3) can be used to determine the OAM is operative. If both registers value 1, then bidirectional OAM communication is operative.
The attached STA may change the register BASE-U OAM enable (3.2348.1) without PMA reset. In such a case, the read values of the register does not longer reflect current status of OAM channel. However, in this case, it is responsibility of the STA to maintain consistency of operations through write operations to the MDIO registers.

*Cl* **45** *SC* **45.2.3.87c.4** *P* **36** *L* **28** # 243

Slavick, Jeff — Broadcom

*Comment Type* **TR** *Comment Status* **R** *Registers effect*

There is no reflection of what the current operating mode of EEE. 3.2348.0 only takes affect after a pmd_reset, so how do you tell if the current state of the enable bit represents the operation state?

*SuggestedRemedy*

Add a new BASE-U EEE status field that relfects the current operating state of EEE mode.

*Response* *Response Status* **U**

REJECT.
EEE capability is managed in MDIO with registers parallel to those used to manage BASE-U OAM. See response to comment #242.

*Cl* **105** *SC* **105.5** *P* **50** *L* **42** # 248

Nicholl, Shawn — AMD

*Comment Type* **TR** *Comment Status* **R** *RS-FEC*

In Table 105-3 "Sublayer delay constraints", the 25GBASE-AU PHY sublayer has maximum delay of 11 264 bit time. This includes contributions from PCS, FEC, PMA, and PMD. In contrast, the same table lists 24 576 bit time as the sublayer maximum delay for just the 25GBASE-R RS-FEC alone.

*SuggestedRemedy*

Propose to update the 25GBASE-AU PHY sublayer delay to a higher value to allow flexibility in the implementation. Propose a value of 32768 bit time (64 pause_quanta) based on a sum of the 25GBASE-R PCS (3584 BT), 25GBASE-R RS-FEC (24576 BT), 25GBASE-R PMA (4096 BT), and 25GASE-*R PMD (512 BT).

*Response* *Response Status* **U**

REJECT.
Delay is specified 25GMII to 25GMII. It considers sum of delays for TX and RX sides of PCS, PMA and PMD sublayers, without including propagation delay of the fiber medium. 11264 bit times corresponds to 2.2x the time needed to transmit a RS-FEC code-word (544 RS symbols, 5440 bits). This upper bound limit has been specified with >25% margin considering actual implementation in a technology node qualified for automotive application.

*Cl* **166** *SC* **166.15** *P* **138** *L* **42** # 249

Nicholl, Shawn — AMD

*Comment Type* **TR** *Comment Status* **R** *RS-FEC*

Update Table 166-23 "Delay constraints) pending resolution of comment against Table 105-3 "Sublayer delay constraints".

*SuggestedRemedy*

If 25GBASE-AU delay contraints is updated in Table 105-3, then make corresponding update in Table 166-23 for 25GBASE-AU. In addition, to retain identical delay constraint for all PHY in Table 166-23, then update other PHY rows to match the new 25GBASE-AU delay constraint value.

*Response* *Response Status* **U**

REJECT.
See #248.